Q.P. Code: 16EC408 **R16**

Reg. No: | | | | | | | | | | |

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR

(AUTONOMOUS)

B.Tech II Year II Semester Supplementary Examinations July-2022

COMPUTER ORGANIZATION AND ARCHITECTURE

(Electronics and Communication Engineering)

Time: 3 hours Max. Marks: 60

(Answer all Five Units **5 x 12 = 60** Marks)

UNIT-I

1	a	Explain the basic components of Generic Computing system regardless of its internalarchitecture with practical real time examples.	L2	6M
	b	Explain the phases involved in Instruction cycle with the help of necessary timing diagrams.	L2	6M

OR

2	a	Identify the crucial features to design the instruction set architecture for a specific purposeprocessor.	L1	6M
	b	Describe the Instruction set Architecture of simple computer.	L2	6M

UNIT-II

3	a	Using the register transfer notations, explain the Memory-Reference instructions with examples.	L2	8M
	b	Elaborate the steps involved in execution of Memory-Reference instructions with its timing signals.	L1	4M

OR

4	a	What is the use of program control instructions? Mention its typical instructions.	L1	6M
	b	Explain in detail about status bit conditions with example.	L2	6M

UNIT-III

5	a	Design Bus system for Four-bit register using 4x1 Mux.	L5	6M
	b	Implement Bus line for an 8-bit register using three state-buffers.	L3	6M

OR

6	a	Design a 4-bit ALU which performs arithmetic, Logical and shift operations.	L5	6M
	b	write about hardware organization of micro programmed control unit.	L1	6M

UNIT-IV

7	a	Discuss the Memory Hierarchy in computer system with regard to Speed, Size and Cost.	L2	6M
	b	Explain about main memory and its types.	L2	6M

OR

8	a	Elaborate how DMA bypasses CPU and speeds up the memory operation.	L2	4M
	b	With a neat schematic, Explain about DMA controller and its mode of data transfer.	L2	8M

UNIT-V

9	a	Implement a simple pipeline unit for floating addition and subtraction.	L4	6M
	b	Consider an adder circuit with delays of four segment as t_1=60 ns, t_2=70 ns,t_3=100 ns,t_4=80 ns and interface resistors have a delay of t_r=10 ns. i) Find the clock cycle for pipeline. ii)Find out clock cycle for non-pipelined adder. iii) Speed up of pipelined over non-pipelined.	L3	6M

OR

10	a	With examples, Explain four segment CPU pipeline and Timing of instruction pipeline.	L2	6M
	b	Elaborate the major difficulties that cause the instruction pipeline to deviate from its normal operation.	L1	6M

*** END ***